

Serial No. 09/730,747  
Amdt. dated **October 6, 2004**  
Reply to Office Action dated July 16, 2004

Docket No. P-162

**REMARKS/ARGUMENTS**

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 2-10 and 12-25 are pending in the present application. Claims 1 and 11 have been canceled, claims 2-8 and 12-16 have been amended and claims 17-25 have been added by the present amendment.

In the outstanding Office Action, claims 11 and 15 were rejected under 35 U.S.C. § 112, second paragraph; claims 1, 11 and 12 were rejected under 35 U.S.C. § 102(e) as anticipated by Hellenthal et al.; claims 3 and 13 were rejected under 35 U.S.C. § 103(a) as unpatentable over Hellenthal et al. in view of Ayaki et al.; and claims 2, 4-10 and 14-16 were indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter. In light of this indication, claims 2 and 14 have been rewritten in independent form. Further, the claims have been amended to correct minor cosmetic informalities and to better correspond with U.S. claim drafting practice. Claims 11 and 15 have also been amended in light of the comments noted in the outstanding Office Action regarding the rejection of these claims under 35 U.S.C. § 112, second paragraph.

Accordingly, it is respectfully submitted independent claims 2 and 14 and each of the claims depending therefrom are allowable.

Further, new claims 17-25 have been added to set forth the invention in a varying scope, and Applicants submit the new claims are supported by the originally filed application.

In particular, new claim 17 is directed to an apparatus for verifying a memory coherence of a duplication processor including an active processor having an active memory, a standby image memory buffer (SMIB) and first and second processors, in which the first processor is configured to issue a standby memory read command to the second processor. Also included is a standby processor having a standby memory. Further, upon receiving the standby memory read command from the first processor, the second processor instructs the standby processor to read data from the standby memory and controls operations to store the data read from the standby memory into the SMIB such that the first processor need only issue the standby memory read command to have data from the standby memory stored into the SMIB.

The feature in which the first processor need only issue the standby memory read command to have data from the standby memory stored in the standby image memory buffer (SMIB) is shown in a non-limiting example in Fig. 2 and is described in the specification at page 12, lines 15-24. On the contrary, Hellenthal et al. does not teach or suggest the claimed second processor that controls operations to store the data read from the standby memory into the SMIB such that the first processor need only issue the standby read

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command to have data from the standby memory stored into the SMIB. Ayaki et al. also does not teach or suggest this feature.

Accordingly, it is respectfully submitted the new claims are also allowable.

### **CONCLUSION**

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney, **David A. Bilodeau**, at the telephone number listed below.

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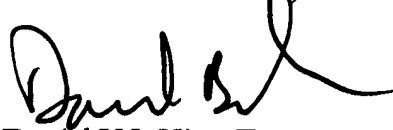
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To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,  
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